10.4: Phased Reset Timing for Improved Digital Micromirror Device™ (DMD™) Brightness

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Abstract

A new DMD™ architecture and operation is described in which the DMD cells are horizontally partitioned into reset groups, each of which is loaded and reset with time phasing. Phased reset operation of reset groups affords a significant improvement in brightness and picture quality by allowing a more efficient pulse width modulation pattern.

Introduction

Figure 1. DMD darkfield projection showing isolated mirror out of the array of mirrors on device

Digital Light Processing™ (DLP™) display systems are based upon the Digital Micromirror Device (DMD™), a spatial light modulator developed at Texas Instruments. The DMD is a CMOS SRAM device with a superstructure array of micromechanical mirrors functionally located over each memory cell. Each aluminum micromirror is 16 μm square and has a separation of 17 μm center-to-center. DLP systems with micromirror arrays up to 2048x1152 have been demonstrated.

The video image is produced by separating high intensity white light into red, green and blue components either coincident through dichroic filters or by time-multiplexing the colors using a color wheel.

Memory cells on the DMD loaded with a logical '1' will position the mirror, through electrostatic forces, such that the incident light is reflected into the aperture of the projection lens using darkfield projection techniques as shown in Figure 1. Memory cells loaded with a logical '0' are positioned such that the incident light is directed away from the projection lens and into a light sink. The 'on' state light is optically recombined with the other color components and projected onto the viewing screen.
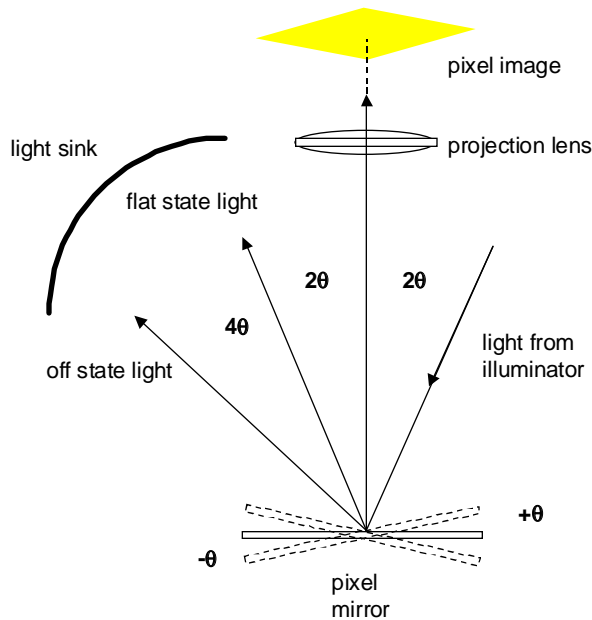
Digital Picture Creation for DLP

Light intensities from the DMD are produced by pulse width modulating (PWM) the mirrors over the operating refresh time. The internal DLP digital (amplitude modulated) video signal is converted to this PWM format.
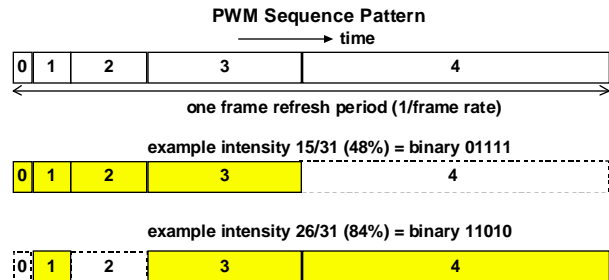

Figure 2. Binary PWM sequence pattern with two examples of how intensity values are generated with the sequence (for simplicity, only 5-bit video is shown here).

In the binary PWM pixel representation, a pixel's LSB consumes $1/(2^n-1)$ of the total refresh period, where n is the number of bits per color. The LSB+1 bit consumes double the LSB time. This pattern continues for all bits of the given pixel. The human visual system effectively integrates the pulsed light to form the perception of desired intensity. The gray scale perceived is proportional to the percentage of time the mirror is "on" during the refresh time.

In practice, the long MSB's shown in Figure 2 are shown in multiple parts by utilizing a technique referred to as *bit-splitting*. This process consists of breaking the duty cycle of longer bits into smaller pieces distributed throughout the refresh time. Bit-splitting can create a more pleasing picture than those shown with contiguous bits. Figure 3 illustrates how this can be implemented for the intensity values in Figure 2.
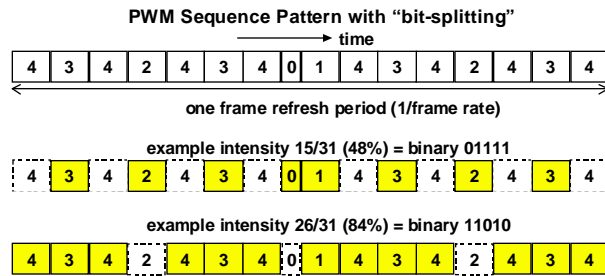
PWM Sequence Pattern with "bit-splitting"

Figure 3. PWM sequence with bit-splitting and two examples of how intensity values are generated with the sequence

DMD Global Reset Operation

Prior to the development described in this paper, the DMD was controlled electronically in a *global* manner, with all cells being addressed and reset simultaneously. While data is being loaded onto the DMD, the mirrors remain in the state corresponding to their previous load due to a bias voltage which is applied to all mirrors. Thus, the bias voltage "holds" all the mirrors in place while the next bit is loaded. After the entire device is loaded with the new data bit plane, the bias voltage is "reset". Thus, all mirrors assume the position corresponding to the new data at the same time.

Figure 4 illustrates the reset and memory operations corresponding to the sequence of Figure 3 and the resulting bit display. While the first bit plane (bit 3) is being displayed, the next bit plane (bit 4) is being loaded. Upon reset, the loaded bit 4 is displayed. Then while bit 4 is displayed the next bit plane (bit 2) is loaded. This continues throughout the entire frame time, during which all bit planes are displayed with their proper weights.
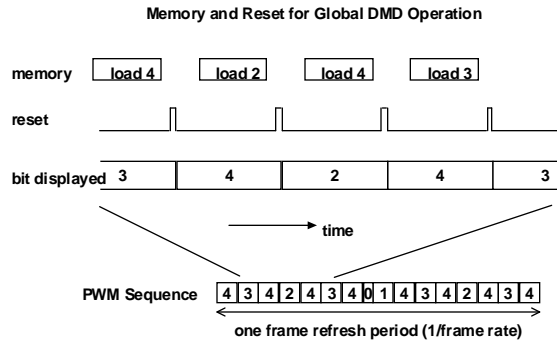
Memory and Reset for Global DMD Operation

Figure 4. Global Reset DMD Operation. A portion of the sequence from Figure 3 is shown here.

A fundamental limitation of this load-reset method occurs when a bit requires a display duration shorter than the time necessary to load the entire device. In this case, a clear-device operation is performed instead of a load. The DMD is designed to perform a full clear (set all memory cells to '0') in a small fraction of the time required to load the entire device. Figure 5 shows the resulting load-reset pattern for such bit planes.

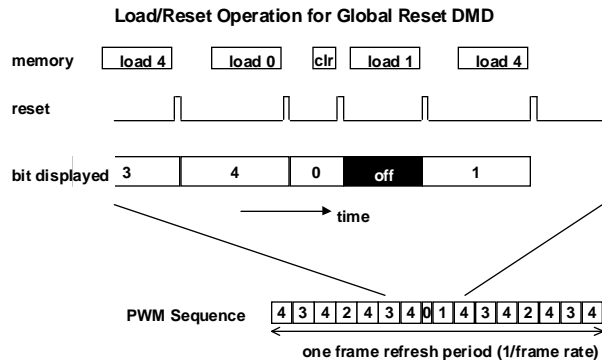**Load/Reset Operation for Global Reset DMD**

Figure 5. Global Reset DMD Operation showing short bit. Notice that a dark time is required during which bit 1 is loaded because bit 0 is too short to accommodate a device load.

Figure 5 illustrates how mirror off time is required for those bit segments which are shorter than a device load time. These forced mirror off times can cause a significant decrease in system brightness. The use of bit-splitting can also be limited by the minimum time needed for an efficient bit segment. Thus, mirror off times contribute directly to a loss of brightness and restrictions on bit-splitting. Both of these conditions are alleviated through the use of a new device architecture and technique called phased reset.
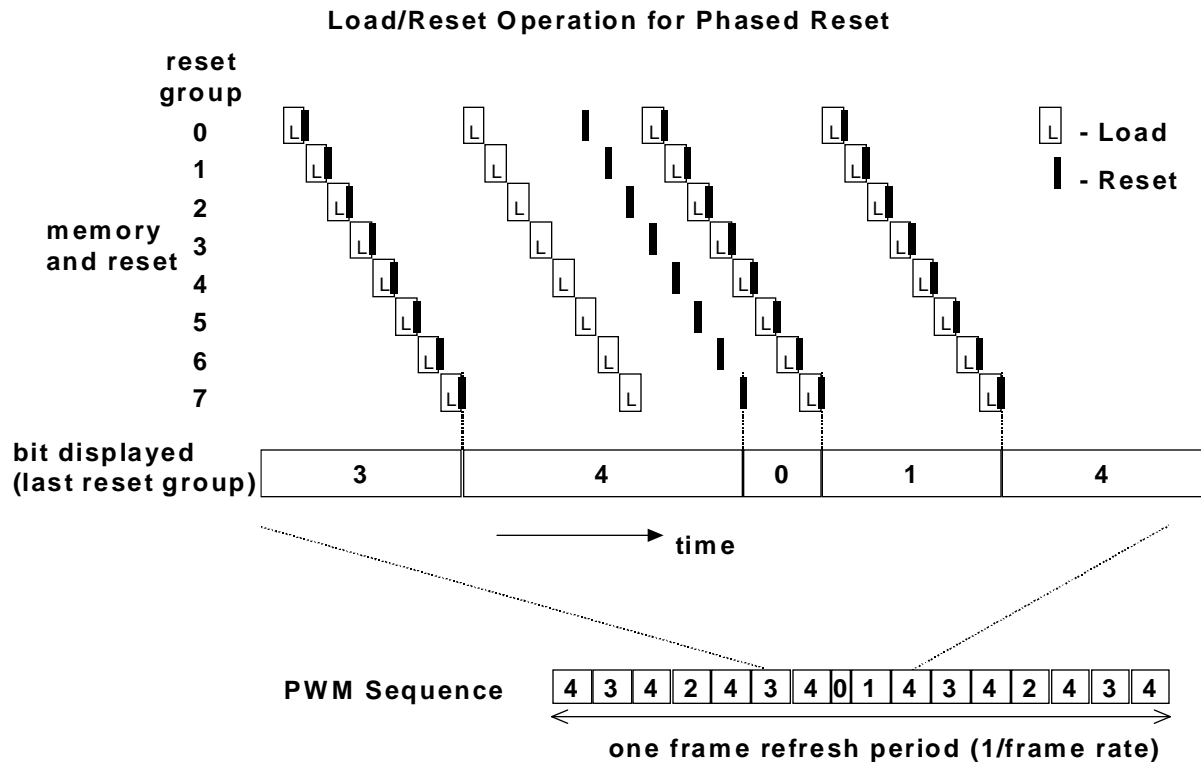
Load/Reset Operation for Phased Reset

Figure 6. Phased reset operation. Each reset group is independently loaded and reset with no need for dark time as in Figure 5.

DMD Phased Reset Operation

For phased reset timing, the DMD is partitioned into horizontal reset groups. For example, the 640x480 active mirrors on a VGA DMD are divided into 12 groups of 640x40 pixels. Two important distinctions are made between global and phased reset DMD operation:

1) Each reset group is loaded and reset independently from other groups.

2) Load and reset operations within a given group are no longer tied together, but may be separated by a period of time. (For global operation, a reset always immediately followed a load)

The phased addressing pattern is shown in Figure 6. In phased operation, each reset group is independently loaded and reset. In the sequence shown, bit 0 is too short to accommodate a full load. Thus, bit 4 time is chosen to be long enough to compensate for an early load of bit 0. Then as bit 1 is loaded, the mirrors are reset. Bit 0 need not fully accommodate a device load because the phased structure allows for the display time of bit 1 to begin immediately as the different groups are loaded.
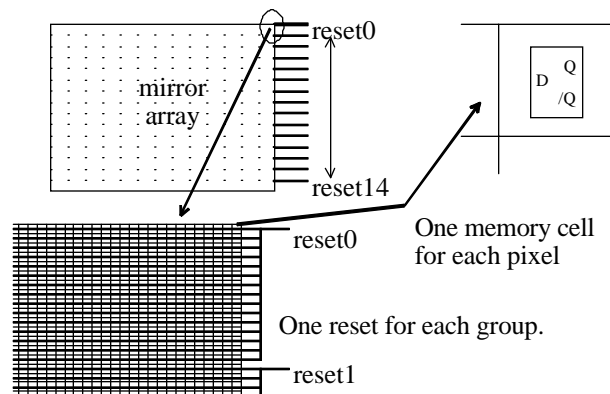
Phased Reset DMD Architecture

Figure 7. Divided reset DMD for phased operation.

A DMD architecture that enables phased reset operation by partitioning the reset groups has been developed. The divided reset structure connects a separate reset line to each individual reset group. The memory is still organized with a single memory cell controlling each mirror. Thus, the reset operation may be performed on

all the mirrors of a single reset group. Figure 7 shows the divided reset DMD architecture.
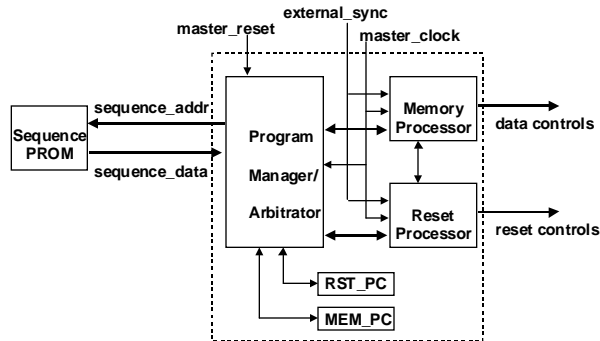
Phased Reset Sequence Controller

Figure 8. Sequence controller design for independently controlling memory and reset DMD operation.

A new PWM sequence controller has been developed which controls the DMD for phased reset operation. This controller incorporates two pseudo-independent control circuits. One supervises loading operations while the other supervises reset operations. In previous global reset DLP systems, a single memory/reset controller was sufficient as load and reset operations were always tied by a fixed delay. As mentioned earlier, phased operation calls for independent control of loads and resets.

The Phased Reset Sequence Controller operates upon two sets of machine code instructions, one specifying the memory operations and one specifying the reset operations. These instructions are stored in the Sequence PROM, which may contain multiple sequences for various input frame rates and application modes.

Phased Reset Sequence Generation

Generation of the sequence program to be written into the sequence PROM is achieved with TIMEGEN, a software package which generates the instruction listing for both memory and reset control of the DMD. TIMEGEN handles all housekeeping necessary in the distribution of bit times to ensure a linear light transfer function for each reset group. Furthermore, it distributes time properly accommodate short bits. TIMEGEN also performs adjustments of the loads and resets where necessary to avoid reset conflict between reset groups.

Conclusions

The phased reset DMD architecture and operation can significantly improve the efficiency of PWM bit sequences in a DLP projection system. This efficiency increase affords gains in two aspects of picture quality:

> 1) brightness due to the removal of dark times required in global systems.

> 2) temporal continuity by allowing more bit-splitting without a brightness penalty.

References

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